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APPENDIX "A"

Semiconductor Memories

A Handbook of Design, Manufacture and Application

Second Edition

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3 TRENDS IN MEMORY APPLICATIONS

3.1 VARIETIES OF DATA STORAGE DEVICES BY MEDIA

Over the years many different media have been tried for the basic data storage function as shown in Figure 3.1. Logical bits have been stored in mechanical devices such as paper tape and cards, in magnetic moving media such as bubbles, hard disks, floppy disks and core, in optical moving media such as magneto–optical disk and holographic devices, and in solid state media which include semiconductors and ferroelectrics. Semiconductors divide by technology into MOS, bipolar and charge coupled devices, and by function into RAM, ROM, and SAM. MOS and bipolar are available in all three functions, while charge coupled devices are available only as SAM.

3.2 FUNCTIONAL CHARACTERISTICS OF VARIOUS SEMICONDUCTOR MEMORIES

The basic differences in function in semiconductor memories have come about as a result of specific requirements of the differing systems applications in which they are used. No single set of memory characteristics is optimal for all systems, nor has any single memory yet been made which has all of the optimum characteristics.

Functional characteristics that are significant for the systems environment include performance (speed), power dissipation (heat), memory density (number of storage bits per chip), chip size (memory cost), size of package (system cost), external organization of the memory, reprogrammability (endurance of the memory to repeated write–erase cycles), long term reliability characteristics, ability to retain data when the power is off (volatility), length of time the data is retained when dc power is on without an active refresh of the data (data retention), interface voltage levels into the system (TTL, ECL, CMOS), optimal power supply voltage levels, moisture resistance (hermeticity) of the package, and the amount of logic integrated on the memory rather than used separately in the system.

There are several major product types of semiconductor memories differing by various sets of these characteristics. This was determined historically by the basic

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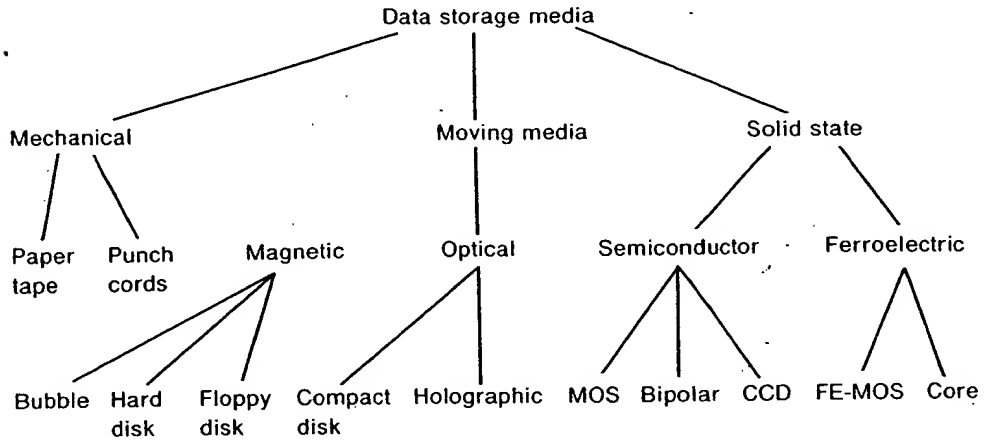

Figure 3.1
Various catagories of data storage devices.

Characteristic	DRAM	SRAM	EPROM	ROM	EEPROM	NVRAM
Number of devices in cell	1.5	4–6	1.5	1.0	2.5	8–9
Relative cell size	1.5	4–6	1.5	1.0	3–4	9–10
Density (1990)	4Mb	1Mb	4Mb	4Mb	1Mb	16k
Overhead cost	yes refresh logic	no	yes UV erase programmer	yes mask charges	no	no
Volatile (power off)	yes	yes	no	no	no	no
Data retention (d.c. power on)	4 ms	∞	10 years	∞	10 years	10 years
In system reprogrammable	yes	yes	no	no	yes	yes
Number of reprogram times (endurance)	∞	∞	100 PROM(1)	0	10 000 –1000 000	10 000 ∞ (write)
Typical write (Reprogram) speed	100 ns	25 ns	30 min	—	2.5 s	—
Typical read speed (ns)	100	25	100	100	200	200
Number of read cycles	∞	∞	∞	∞	∞	∞

Figure 3.2
Characteristics of MOS memory product types.

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memory cell. Semiconductor memories are split by major cell type into DRAMs, SRAMs, SAMs, EPROMs, EEPROMs, and ROMs. General characteristics of the basic MOS memory types are shown in Figure 3.2. Minor variations include the NVRAM and the CAM.

The structure of the memory array and periphery determines the input and output organization. The logic in the periphery also determines functional subcategories of memories such as video and multi-port DRAMs, synchronous and asynchronous SRAMs.

A further subset is defined by the Input and Output (I/O) levels and configuration of the memory. I/O levels can be TTL, ECL, or CMOS. Inputs, outputs, and addresses can be multiplexed or non-multiplexed, serial or parallel.

3.2.1 MOS memory selection by system requirement

Different systems require different MOS memory characteristics. For example, a memory system requiring an infinitely reprogrammable memory would use an SRAM or a DRAM. If it is a large memory system with commercial cost pressure then it will use the highest density, lowest cost option—the DRAM. If it is a large very fast system requiring a random read access memory, then it will either use SRAM for the main memory or have a small SRAM cache which can make a lower cost but slower DRAM memory appear faster in the system. If it is important that the main memory not lose its data when the power fails, there are again several options. Either SRAM can be used for the main memory due to its low standby power dissipation and backed up by a battery, or the main memory can be backed up by an EEPROM.

As another example a system which needs a small quantity of fast infinitely writable non-volatile memory will use an NVRAM, bearing in mind that its non-volatile reprogrammability is the same as the EEPROM—about 10 000 reprogram cycles.

In general DRAMs and EPROMs tend to be optimized for high density and low cost and used in large systems where many parts need to be assembled in a small space. The large quantity of parts used mean that the per-unit overhead costs are low.

DRAMs have the lowest cost of any RAM and the highest density because they have the smallest memory cell, consisting of one transistor and a capacitor. The capacitor stores the charge when the memory is in the '1' state. The capacitor occupies a large percentage of the room in the memory cell. In high density DRAMs it is usually either stacked on top of the transistor or lowered into a narrow trench in the silicon. A DRAM, therefore, effectively has a one plus transistor cell area.

The penalty that is paid for this small cell size and consequent high density is the need for the memory system to provide a periodic refresh to the cell to restore the charge to the capacitor as it leaks away. During the time that the memory cell is being 'refreshed' no other operation can take place in that area of the array. This 'dead time' slows down the effective speed of the DRAM in the system. While the percentage of the operating time that is occupied with refresh is decreasing as higher quality capacitors are constructed, refresh is still a significant factor in the timing of the system.

All of the capacitors in the memory array must be periodically refreshed. This is done by accessing each row in the array, one row at a time. When a row is accessed,

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